

Abstract

The present invention relates to a composite memory device comprising first through third memory devices, a
5 memory bus, and first through third memory controllers. The first memory device is an asynchronous memory device, the second memory device is a synchronous memory device configured to operate in a page mode, and the third memory device is a synchronous memory device configured to operate
10 in a burst mode. The first through the third memory controllers are configured to control data transfer operation between the memory bus and the first through the third memory devices, respectively. The first through the third memory devices are controlled by an external memory
15 controller to exchange data with an external system bus, and when one of the first through the third memory devices exchanges data with the external system bus, the rest two memory devices are allowed to exchange data via the memory bus.

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